

August 1998

54ACTQ273

Quiet Series Octal D Flip-Flop

General Description

The ACTQ273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) input load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

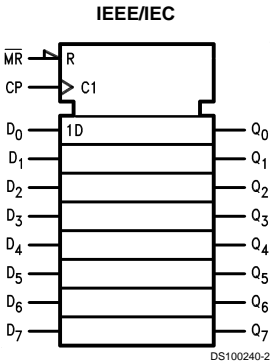
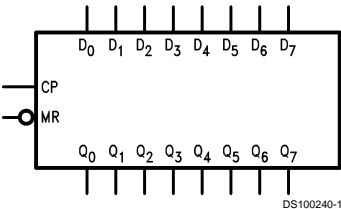
The ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold

performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- I_{CC} reduced by 50%
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity
- Buffered common clock and asynchronous master reset
- Outputs source/sink 24 mA
- Faster prop delays than the standard 'AC/ACT273
- 4 kV minimum ESD immunity
- Standard Microcircuit Drawing (SMD) 5962-89735

Logic Symbols

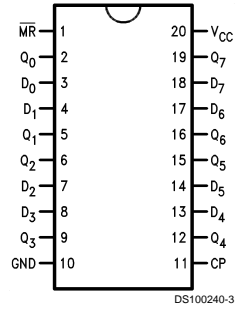


Pin Names	Description
D_0-D_7	Data Inputs
\overline{MR}	Master Reset
CP	Clock Pulse Input
Q_0-Q_7	Data Outputs

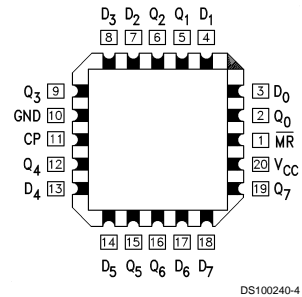
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FACT Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

Pin Assignment
for DIP and Flatpak



Pin Assignment
for LCC



Mode Select-Function Table

Operating Mode	Inputs			Outputs
	MR	CP	D _n	Q _n
Reset (Clear)	L	X	X	L
Load "1"	H	↗	H	H
Load "0"	H	↘	L	L

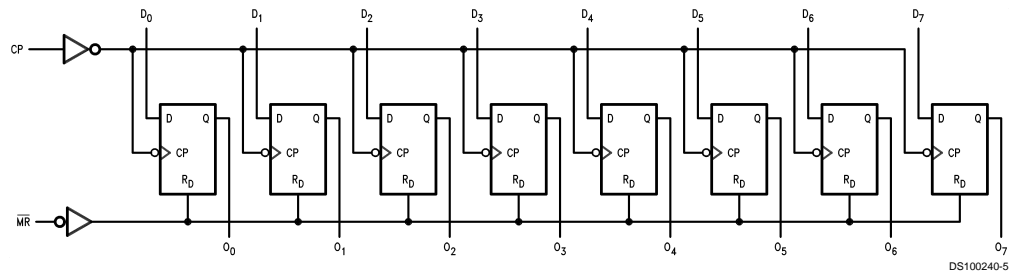
Note 1: H = HIGH Voltage Level

Note 2: L = LOW Voltage Level

Note 3: X = Immaterial

Note 4: ↗ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	–0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	–20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	–0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	–20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	–0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	–65°C to +150°C

DC Latch-up Source or

Sink Current ±300 mA

Junction Temperature (T_J)

CDIP 175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACTQ	–55°C to +125°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 5: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 6: All commercial packaging is not recommended for applications requiring greater than 2000 temperature cycles from –40°C to +125°C.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ	Units	Conditions
			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
			Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.7	V	(Note 7) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
		5.5	4.7		
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 7) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
		5.5	0.50		
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, \text{GND}$
I_{CCT}	Maximum I_{CC} /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
I_{OLD}	Minimum Dynamic Output Current (Note 8)	5.5	50	mA	$V_{OLD} = 1.65V \text{ Max}$
I_{OHD}		5.5	–50	mA	$V_{OHD} = 3.85V \text{ Min}$
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	$V_{IN} = V_{CC}$ or GND (Note 9)

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54ACTQ	Units	Conditions
			T _A = -55°C to +125°C		
			Guaranteed Limits		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0	1.5	V	(Note 10)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0	-1.2	V	(Note 10)

Note 7: All outputs loaded; thresholds on input associated with output under test.

Note 8: Maximum test duration 2.0 ms, one output loaded at a time.

Note 9: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ @ 25°C.

Note 10: Max number of outputs defined as (n). n - 1 Data inputs are driven 0V to 3V; one output @ GND.

Note 11: Max number of Data Inputs (n) switching. (n - 1) Inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}) f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 12)	54ACTQ	Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF		
			Min Max		
f _{max}	Maximum Clock Frequency	5.0	85	MHz	
t _{PHL} , t _{PLH}	Propagation Delay Clock to Output	5.0	1.5 10.0	ns	Figure 4
t _{PHL}	Propagation Delay MR to Output	5.0	1.5 11.0	ns	Figure 4

Note 12: Voltage Range 5.0 is 5.0V ±0.5V.

AC Operating Requirements

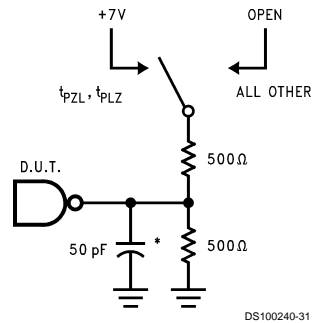
Symbol	Parameter	V _{CC} (V) (Note 13)	54ACTQ	Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF		
			Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW Data to CP	5.0	5.0	ns	Figure 6
t _h	Hold Time, HIGH or LOW Data to CP	5.0	2.0	ns	Figure 6
t _w	Clock Pulse Width HIGH or LOW	5.0	5.0	ns	Figure 5
t _w	MR Pulse Width HIGH or LOW	5.0	5.0	ns	Figure 5
t _{rec}	Recovery Time MR to CP	5.0	4.0	ns	Figure 6

Note 13: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.0V$

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

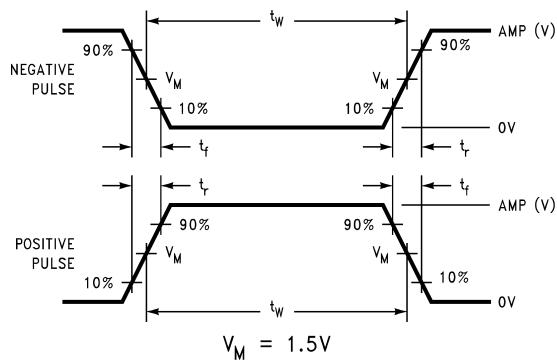


FIGURE 2. Test Input Signal Levels

Amplitude	Rep.Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

AC Waveforms

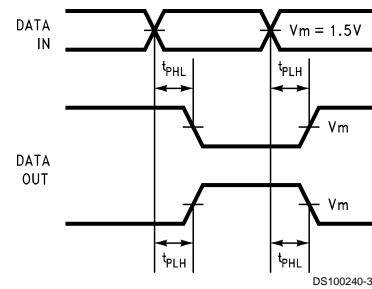


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

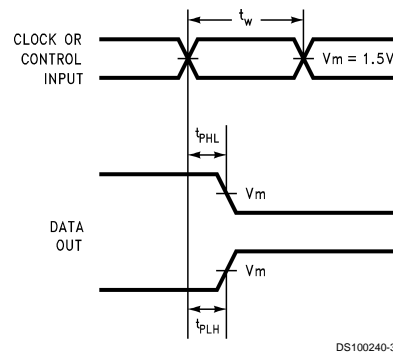


FIGURE 5. Propagation Delay, Pulse Width Waveforms

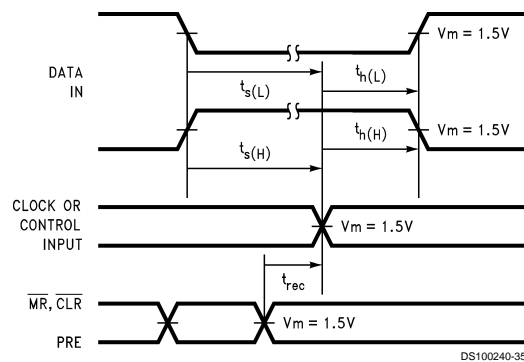
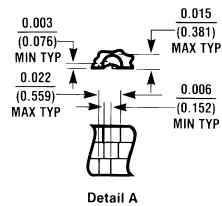
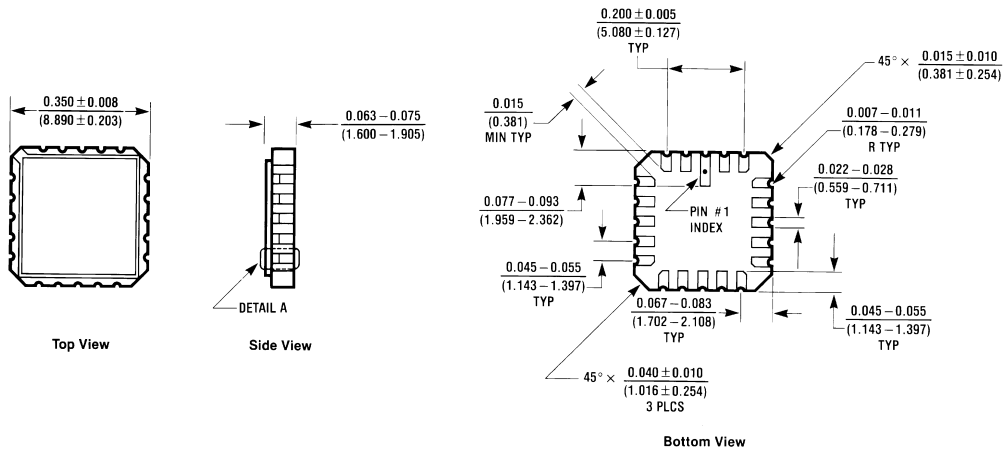


FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

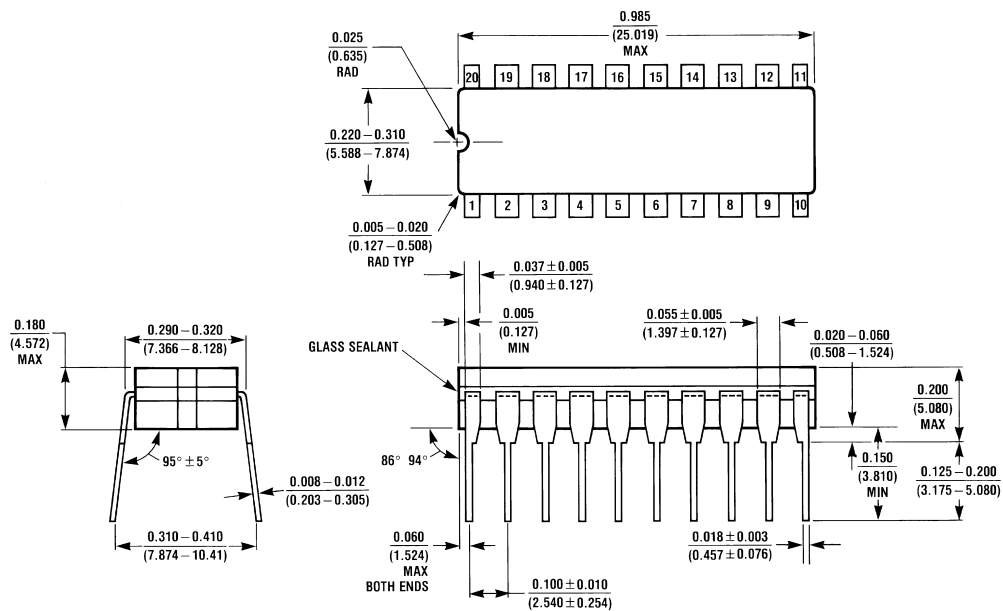


Physical Dimensions inches (millimeters) unless otherwise noted



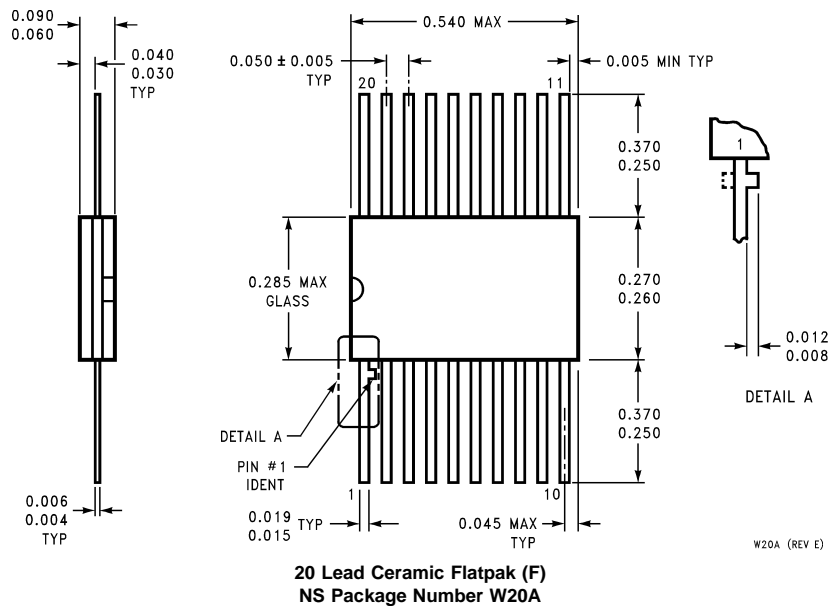
E20A (REV D)

20-Terminal Ceramic Leadless Chip Carrier (L) NS Package Number E20A



J20A (REV M)

20-Lead Ceramic Dual-In-Line Package (D) NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)**LIFE SUPPORT POLICY**

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